REMARKS

Claims 1-22, 27-44, and 49 are currently pending in the application. Claims 1-22, 27-44, and 49 were rejected.

The Examiner maintained the rejection claims 1-14, 20, 22, 27-32, 34, 35, 37-42, 44, and 49 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,488,729 (Vegesna) in view of U.S. Patent No. 5,920,899 (Chu). The Examiner also rejected claims 15-19, 21, 33, 36, 43, and 45-48 under 35 U.S.C. 103(a) as being unpatentable over the combination of Vegesna and Chu in view of a variety of other references. The rejections are respectfully traversed.

As acknowledged by the Examiner's withdrawal of the previous grounds of rejection, the claims of the present application are clearly distinguishable from the system described in Vegesna in a number of respects which have been made of record in the previous responses, the arguments of which are incorporated herein by reference. In addition, the Examiner's combination of Vegesna and Chu is not appropriate and, as such, any rejections based thereon should be withdrawn.

As discussed in previous responses, a key aspect of the approach described in Vegesna is that instructions are issued to its parallel pipelines simultaneously. See, for example, column 1, lines 16-22; column 2, lines 56-61 and 64-67; column 3, lines 11-13; column 14, lines 59-61; column 23, lines 8-11; column 29, lines 34-37; etc. In fact, because Vegesna's architecture is controlled by a clock signal, units of data can only be issued to its pipelines on a clock transition, and can therefore only be issued to the pipelines simultaneously. See for example, the various figures relating units of data to clock cycles. And because the synchronous parallel pipelines process parallel data units simultaneously, elaborate measures are required to determine whether there are any dependencies between the data units and, if any are found, manipulate the flow of one or both pipelines to handle the dependency. As is well known, this is extremely expensive in chip resources and severely limits the scale and efficiency of N-way synchronous pipelines.

Chu, on the other hand, describes an "asynchronous pipeline that is divided into separate data and signal chains by moving the data register load signal buffer outside of the closed loop that generates the output request event from the input request event." This causes "the output request event to occur before output data is available." See Abstract. Significantly, and as is clear throughout the specification and drawings, Chu only describes the design and operation of a single pipeline (see, for example, FIGs. 7 and 15-17), and provides no teachings or suggestions as to how to implement multiple instances of his pipeline in parallel.

The combination of the teachings of Vegesna and Chu as proposed by the Examiner must fail for a number of reasons. First, replacing each of the synchronous pipelines of Vegesna with an instance of the asynchronous pipeline of Chu would require some form of translation circuitry between synchronous domain embodied by the context in which Vegesna's pipelines are implemented, and the asynchronous domain embodied by each instance of Chu's pipeline. No such translation circuitry is taught or suggested.

Second, virtually all of the circuits designed for use with Vegesna's pipelines would need to be either significantly altered or completely replaced to make them compatible with the manner in which Chu's pipeline operates. For example, Vegesna's Intrapacket Scheduling Logic 76 and Interpacket Scheduling Logic 78 detect data dependencies within and between packets are both designed to operate in the synchronous domain and on the assumption that the pipelines with which they are interacting are synchronous pipelines to which data are simultaneously issued. The replacement of Vegesna's synchronous pipelines with instances of Chu's asynchronous pipeline would therefore necessitate a complete redesign of each of these circuits as they would not be operable with Chu's pipeline. These are merely two examples of the many circuits in Vegesna for which this is the case.

Third, the Examiner's proposed combination of Vegesna and Chu completely ignores the problem being solved by Vegesna and the manner in which it is solved. As discussed, Vegesna

makes it clear that the solution being proposed to the problem of issuing multiple instructions per clock cycle requires the simultaneous issuance of instructions to its pipelines. This feature of Vegesna's solution is stressed as critical because it is necessitated by the constraints of the context in which the solution is implemented, i.e., a synchronous domain controlled by a clock signal. It therefore strains credibility for the Examiner to suggest that one of skill in the art would attempt to incorporate an asynchronous pipeline in this context as this would not only ignore the main thrust of Vegesna's approach, but would introduce an entirely new set of technical problems for which neither of the references provides any guidance. Thus, the teaching of the references are incompatible.

Even in the unlikely event that one were able to overcome the aforementioned obstacles and successfully combine the teachings of Vegesna and Chu, important limitations recited in the claims of the present application are still neither taught nor suggested by the combination. That is, for example, claim 1 of the present application explicitly recites that "data units are issued to the respective pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time." This limitation is neither taught nor suggested by the cited references either alone, or in combination with each other.

The Examiner points to columns 3-5 and various unrelated figures in Chu to support the assertion that this limitation is shown. However, as discussed above, Chu *cannot* show this limitation in that Chu only describes the design and operation of a single asynchronous pipeline. The passages to which the Examiner refers merely describe the passage of data between *serially* arranged stages in a *single* pipeline. This is clearly irrelevant to the claim limitation to which the Examiner is referring.

Because the combination of the Vegesna and Chu reference is not supportable, and because important limitations in the claims of the present application are not present in either of the references, the rejection of claim 1 should be withdrawn. In addition, the rejection of claims

2-22, 27-44, and 49 should also be withdrawn for at least the reasons discussed.

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (510) 663-1100.

Respectfully submitted,
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